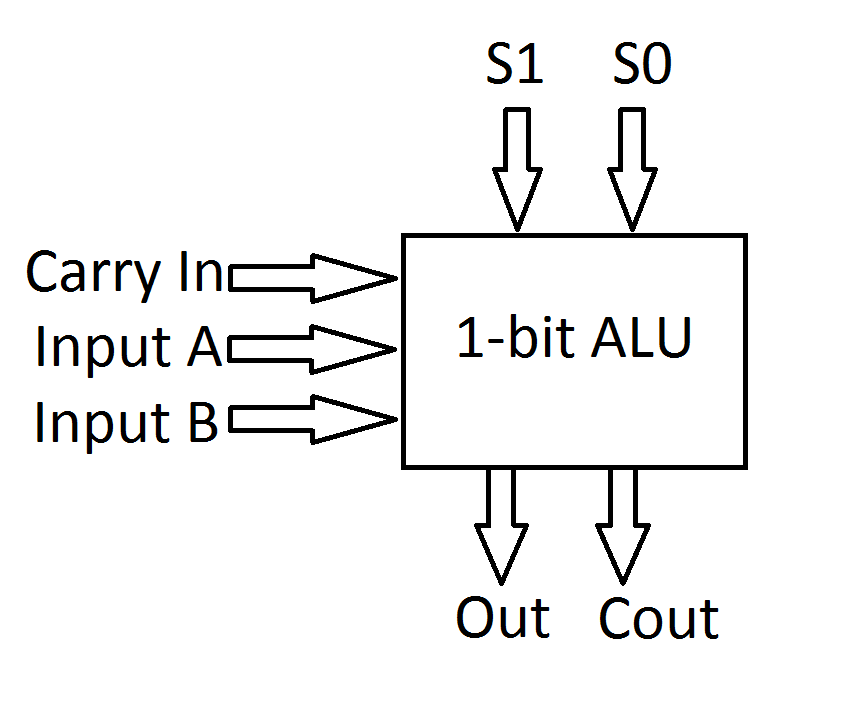
Sumant Sakhalkar

ECE451 Lab 2: 3-bit ALU in Verilog

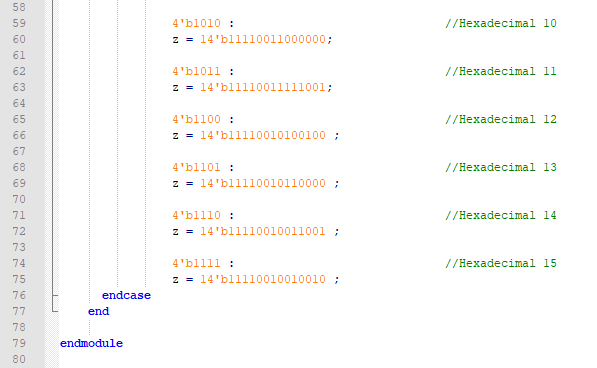
Digital System Design

**Objective:** To learn the basic logic synthesis steps by synthesizing a 3-bit Arithmetic Logic Unit (ALU) using Verilog.

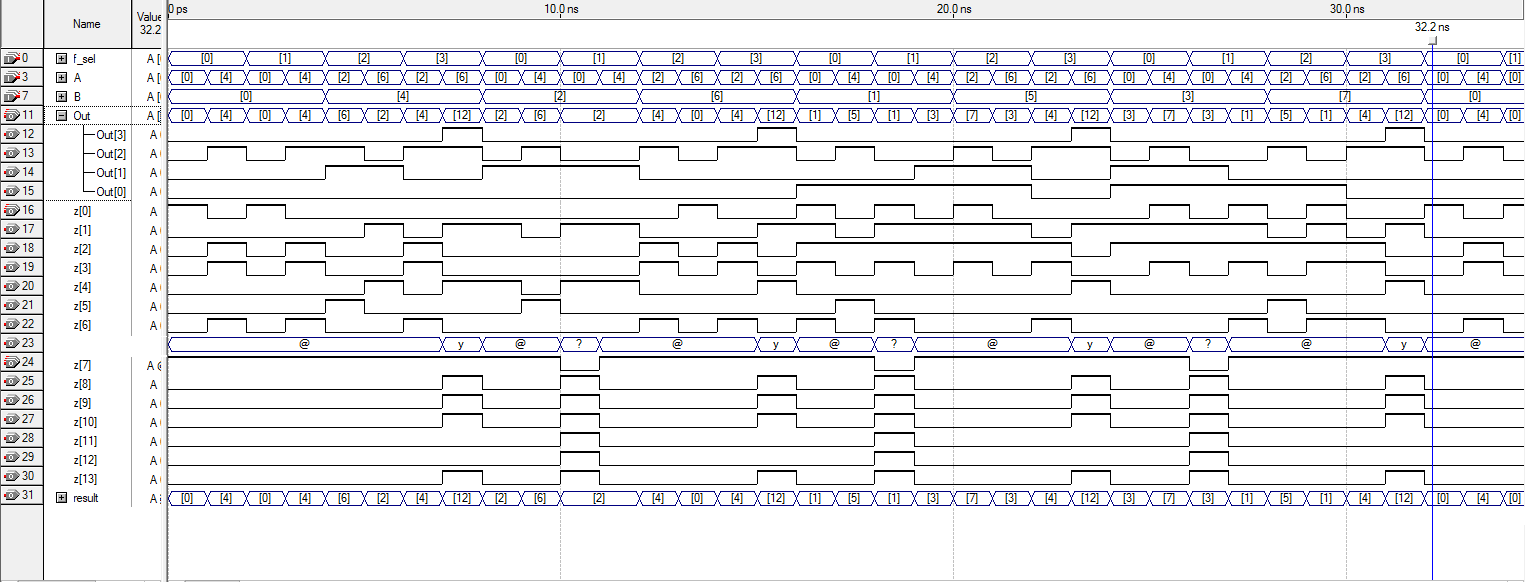
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|  |  |  |
| --- | --- | --- |
| S1 | S0 | Function |
| 0 | 0 | ADD |
| 0 | 1 | SUBTRACT |
| 1 | 0 | XOR |
| 1 | 1 | Left Shift |

**Verilog Code:**



**WAVEFORMS:**



Advantages of Hardware Description Language:

* Can model hardware perfectly
* Can be used to design extremely complex circuits.
* Captures timing information
* Uses concurrent programming in their ability to model multiple parallel processes (such as flip-flops and adders) that automatically execute independently of one another.
* HDLs are well suited for architecture exploration as architectural modifications can be easily evaluated with little concern for signal-level implementation issues.